DETAILED ACTION

RCE

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/20/2009 has been entered.

Response to RCE

2. The information disclosure statement (IDS) submitted on 10/20/2009 was filed after the mailing date of the Notice of Allowance on 07/27/2009. Accordingly, the information disclosure statement is being considered by the examiner.

Examiner's Amendments

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR

1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Hisahi D. Watanabe on July 16, 2009.

The application has been amended as follows:

Claims:

1. (Currently Amended) A method in a packet switched data transfer system for processing header bits and payload bits in a frame of bits, the method comprising:

classifying at a data transfer device each of the header bits in the frame into a first predetermined class of bits and into a second predetermined class of bits based upon a location of the header bit in the frame of bits;

classifying at the data transfer device each of the payload bits in the frame into the first predetermined class of bits and into the second predetermined class of bits based upon a location of the payload bit in the frame of bits;

processing at the data transfer device the first predetermined class of bits, in the frame, in accordance with a first predetermined mechanism; and

processing at the data transfer device the second predetermined class of bits, in the frame, in accordance with a second predetermined mechanism.

2. (Currently Amended) The method of claim 1, further comprising:

constructing at the data transfer device a new frame of bits based upon the processed first predetermined class of bits and the processed second predetermined class of bits.

4. (Currently Amended) A method in a packet switched data transfer system for processing header bits and payload bits in a frame of bits, the method comprising:

classifying at a data transfer device each of the header bits in the frame into a first predetermined class of bits and into a second predetermined class of bits based upon a pre-assigned header weight of the header bit;

classifying at the data transfer device each of the payload bits in the frame into ~~a~~ the first predetermined class of bits and into ~~a~~ the second predetermined class of bits based upon a pre-assigned payload weight of the payload bit;

processing at the data transfer device the first predetermined class of bits, in the frame, in accordance with a first predetermined mechanism; and

processing at the data transfer device the second predetermined class of bits, in the frame, in accordance with a second predetermined mechanism.

5. (Currently Amended) The method of claim 1, wherein:

processing at the data transfer device the first predetermined class of bits in accordance with the first predetermined mechanism includes grouping the first predetermined class of bits; and

processing at the data transfer device the second predetermined class of bits in accordance with the second predetermined mechanism includes grouping the second predetermined class of bits.

6. (Currently Amended) The method of claim 1, further comprising:

grouping at the data transfer device the processed first predetermined class of bits;

grouping at the data transfer device the processed second predetermined class of bits; and

constructing at the data transfer device a new frame of bits based upon the grouped-processed first predetermined class of bits and the grouped processed second predetermined class of bits.

Allowable Subject Matter

4. With respect to the prior art in the IDS, namely Kim, "Proposed Work Item for Radio Optimisation Impacts on PS Domain Architecture," on December 17-20, 2001, the presented claims are allowable over the prior art because the presented prior art merely teaches an outline of radio optimization impacts on PS domain architecture without teaching classifying bits in the

header and payload of a packet.

5. The following is an examiner's statement of reasons for allowance:

Regarding Claims 1, 4, 15 and 17, prior art fails to show alone or in combination the outing queue step of classifying header bits based upon a location of the header bits in the frame; payload bits based upon a location of the payload bits in the frame; header bits based upon a pre-assigned header weight of the header bits; payload bits based upon a pre-assigned header weight of the payload bits. It is noted that the presented prior art in the IDS, fail to disclose or render obvious the above limitations as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Regarding Claims 2, 5, 6, 7, 18 and 19 are allowable because they are dependent claims following the allowable independent claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to WEI-PO KAO whose telephone number is (571)270-3128. The examiner can normally be reached on Monday through Friday, 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571)272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ricky Ngo/

Supervisory Patent Examiner, Art Unit 2464

/Wei-po Kao/

Examiner, Art Unit 2464